IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Abbey, et al.	Docket No.:	ROC920030219US1
Serial No.:	10/624,352	Group Art Unit:	2188
Filed:	07/22/03	Examiner:	DOAN, DUC T.

For: APPARATUS AND METHOD FOR AUTONOMICALLY DETECTING RESOURCES IN A LOGICALLY PARTITIONED COMPUTER SYSTEM

REPLY BRIEF

Mail Stop APPEAL BRIEF - PATENTS
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir/Madam:

This Reply Brief is filed in response to the first Examiner's Answer dated 09/14/2006 and the second Examiner's Answer dated 10/19/2006.

STATUS OF CLAIMS

In the Examiner's Answer, the rejection of claims 37, 40-41, 43-44 and 47-48 under 35 U.S.C. §101 was withdrawn. As a result, the only rejection remaining in this case is the rejection of claims 7-9, 11-14, 21-23, 25-28, 37, 40-41, 43-44 and 47-48 under 35 U.S.C. §102(b) as being anticipated by U.S. Patent Application Publication US 2002/0052914 to Zalewski *et al.* (hereinafter "Zalewski"). The claims remaining in the case are claims 7-9, 11-14, 21-23, 25-28, 37, 40-41, 43-44, and 47-48, all of which stand finally rejected. No claim has been allowed.

ARGUMENT

Issue 2: Whether claims 7-9, 11-14, 21-23, 25-28, 37, 40-41, 43-44 and 47-48 are anticipated under 35 U.S.C. §102(b) by Zalewski

Appellant stands on the arguments made in the Appeal Brief, which are incorporated herein by reference. These additional arguments are made specifically to refute the examiner's allegations in the Examiner's Answer.

In maintaining the rejection of these claims, the examiner makes several statements that show conclusively that Zalewski does not anticipate each and every limitation in these claims under 35 U.S.C. §102(b). Each of the claims in this group is addressed below.

Claims 7-9, 21-23, 37 and 40-41

At page 6, paragraph (A) of the Examiner's Answer, the examiner cites to the status bits in Zalewski and states:

> By monitoring these bits (these statuses [sic] bits), one can easily [sic] "detecting when at least one required resource for the selected logical partition is not powered up" as claimed.

The express teachings of Zalewski and the examiner's own characterization of Zalewski show conclusively that Zalewski presumes a CPU in a slot is powered up, and therefore available. Paragraph [0057] of Zalewski states:

> Each HWRPB which is created by the console program will contain a CPU slot-specific database for each CPU that is in the system, or that can be added to the system without powering the entire system down. **Each CPU that is physically present will be marked "present"**, but only CPUs that will initially execute in a specific partition will be marked "available" in the HWRPB for the partition. (emphasis added)

The language in bold above shows that each CPU that is physically present will be marked "present." If a CPU is present, it may be allocated to a logical partition in Zalewski. Thus, a CPU that is physically present is also presumed in Zalewski to be powered on. By monitoring the status bits in Zalewski, one can easily detect when a CPU is present and powered up (if the bit is a one), or is not present (if the bit is a zero). Nowhere does Zalewski teach or suggest that a CPU can be present but not powered up. For this reason, Zalewski does not teach or suggest "detecting when at least one required resource for the selected logical partition is not powered up" as claimed.

In the Examiner's Answer at paragraph (B) from pages 6-8, the examiner attempts to justify the rejection, but this attempt is unsuccessful. In the first place, the examiner alleges for the first time in the Examiner's Answer that the claim limitation "initiating power up of the at least one required resource that is not powered up" does not have support in the disclosure. The examiner then goes through a very lengthy and convoluted discussion on pages 7 and 8 that is completely irrelevant. Basically the examiner attempts to justify the rejection of these claims by quoting what appellant's specification teaches, and equating the teachings of Zalewski to the teachings in appellant's specification. This is very strange given the express language in the claim that the examiner completely ignores because it allegedly does not have support in the specification.

The examiner alleges the limitation "initiating power up of the at least one required resource that is not powered up" does not have support in the disclosure. The examiner's contention is incorrect. This limitation has clear support at step 382 in FIG. 3,

and p. 12 lines 18-19 of the specification. Because this limitation has clear support in the specification, the examiner's arguments on pages 7 and 8 are completely off the mark and irrelevant. Essentially the examiner looks to a part of the specification, finds teachings in Zalewski that apparently read on the functions in the specification, and concludes the rejection is proper. This is a strange conclusion, indeed, when the actual claim limitation has not been addressed.

Appellant reiterates the argument made so aptly in the Appeal Brief: nowhere does Zalewski teach or suggest initiating power up of at least one required resource that is not powered up. The examiner has provided no argument or rationale or cite to Zalewski that supports the rejection. Because Zalewski does not teach or suggest initiating power up of the at least one required resource that is not powered up, claims 7-9, 21-23, 37 and 40-41 are allowable over Zalewski. Appellant respectfully requests the examiner's rejection of claims 7-9, 21-23, 37 and 40-41 be reversed.

The examiner makes an argument at paragraph (C) on p. 8 of the Examiner's Answer. It is not clear why the examiner made this argument or its relevance to the pending claim limitations. For this reason, appellant dismisses the examiner's argument at paragraph (C) as irrelevant, and does not address this argument in this Reply Brief.

The examiner's argument at paragraph (D) on p. 9 of the Examiner's Answer states:

> Applicant then leaps to the conclusion that Zalewski does not teach "detecting when at least one required resource for the selected logical partition is not powered up." In contrast, Zalewski indicates the CPU resource can be plugged in and powered up, the physical present [sic] of this CPU is thus detected by the setting of the Present bit (see rationale in items A,B).

Appellant respectfully asserts it is the examiner, not appellant, who is leaping to conclusions. The examiner's own language characterizing Zalewski shows this leap of logic by the examiner. Zalewski does indeed teach a CPU can be plugged in and powered up. Once plugged in and powered up, the CPU may be detected by reading the Processor Present bit. However, neither of these steps reads on the limitation in the claims of "detecting when at least one required resource for the selected logical partition is not powered up." Appellant readily admits that when the Processor Present bit in Zalewski is one, this indicates a CPU that is both present and powered on. But when the Processor Present bit is zero, Zalewski cannot assume, as stated by the examiner, that the corresponding CPU not powered up. Indeed, when the Processor Present bit is zero in Zalewski, this means the CPU is not even present. This is supported by the examiner's own characterization of Zalewski at p. 8, second paragraph, of the Examiner's Answer, which states:

> In a similar manner, Zalewski's paragraph 57 discloses when a resource CPU is plugged into a slot (being powered up), the console program detects and setting the CPU present bit.

Because the examiner's own characterization of Zalewski requires the CPU to be plugged into a slot and powered up before the console program detects and sets the corresponding processor present bit, this expressly teaches away from detecting when at least one required resource for the selected logical partition is not powered up, as recited in the pending claims. Thus, it is the examiner who has leaped to the conclusion that Zalewski teaches the limitation "detecting when at least one required resource for the selected logical partition is not powered up." Appellant has conclusively shown by the discussion above that Zalewski teaches an absence of a CPU when the Processor Present bit is zero, and therefore does not teach "detecting when at least one required resource for the selected logical partition is not powered up" as recited in the pending claims.

For the many reasons given above, claim 7 is allowable over Zalewski. Appellant respectfully requests the examiner's rejection of claim 7 under 35 U.S.C. §102(b) be reversed.

In paragraph (E) on p. 9 of the Examiner's Answer, the examiner correctly notes a typographical error in the Appeal Brief. Appellant thanks the examiner for noting this error. The corrections to these two paragraphs are provided below.

Claims 21 and 37 contain limitations similar to those in claim 7, which are addressed in detail above and in the Appeal Brief. As a result, claims 21 and 37 are allowable for the same reasons given above and in the Appeal Brief for claim 7.

Claims 8-9, 22-23 and 40-41 depend on claims 7, 31 and 37, respectively, which are allowable for the reasons given above and in the Appeal Brief. As a result, claims 8-9, 22-23 and 40-41 are allowable as depending on allowable independent claims.

Claims 11-14, 25-28, 43-44 and 47-48

In the Examiner's Answer, the examiner did not address any of appellant's arguments with respect to claims 11-14, 25-28, 43-44 and 47-48 on p. 15-16 of the Appeal Brief. Appellant stands on the arguments made in the Appeal Brief with respect to these claims. In these arguments, appellant challenged the examiner to provide a single operating system operator command that allows powering down a CPU. The examiner has not met this challenge. As stated so aptly in the Appeal Brief, Zalewski does not teach or suggest a resource detection mechanism that initiates power off of a plurality of resources owned by the selected logical partition in response to the selected logical partition being powered off. As a result, all of claims 11-14, 25-28, 43-44 and 47-48 are allowable over Zalewski, as explained in detail in the Appeal Brief.

CONCLUSION

Claims 7-9, 11-14, 21-23, 25-28, 37, 40-41, 43-44, and 47-48 are addressed in this Appeal. For the numerous reasons articulated above, appellant maintains that the rejection of claims 7-9, 11-14, 21-23, 25-28, 37, 40-41, 43-44, and 47-48 under 35 U.S.C. §102(b) is erroneous.

Appellant respectfully submits that this Reply Brief fully responds to, and successfully contravenes, every argument made in the Examiner's Answer in support of the pending rejections. Appellant respectfully requests that the final rejection be reversed and that all claims in the subject patent application be found allowable.

Respectfully submitted,

/derekpmartin/
Derek P. Martin
Reg. No. 36,595

MARTIN & ASSOCIATES, L.L.C.
P.O. Box 548
Carthage, MO 64836-0548
(417) 358-4700
Fax (417) 358-5757